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Readout of two-kilopixel transition-edge sensor arrays for Advanced ACTPol

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ABSTRACT

Advanced ACTPol is an instrument upgrade for the six-meter Atacama Cosmology Telescope (ACT) designed to measure the cosmic microwave background (CMB) temperature and polarization with arcminute-scale angular resolution. To achieve its science goals, Advanced ACTPol utilizes a larger readout multiplexing factor than any previous CMB experiment to measure detector arrays with approximately two thousand transition-edge sensor (TES) bolometers in each 150 mm detector wafer. We present the implementation and testing of the Advanced ACTPol time-division multiplexing readout architecture with a 64-row multiplexing factor. This includes testing of individual multichroic detector pixels and superconducting quantum interference device (SQUID) multiplexing chips as well as testing and optimizing of the integrated readout electronics. In particular, we describe the new automated multiplexing SQUID tuning procedure developed to select and optimize the thousands of SQUID parameters required to readout each Advanced ACTPol array. The multichroic detector pixels in each array use separate channels for each polarization and each of the two frequencies, such that four TESes must be read out per pixel. Challenges addressed include doubling the number of detectors per multiplexed readout channel compared to ACTPol and optimizing the Nyquist inductance to minimize detector and SQUID noise aliasing.

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1. INTRODUCTION

Large arrays of low-temperature detectors are finding increasingly wider use in the detection of radiation, from photons in the sub-mm and gamma-rays, to neutrinos, and even dark matter. In Cosmic Microwave Background (CMB) and sub-mm astronomy, large arrays of detectors permit substantial improvements in sensitivity and mapping speed if the individual detectors are limited by the photon noise background. The most mature superconducting detector technology, the transition-edge sensor (TES),¹ has demonstrated background limited performance across a range of bands and platforms. The present generation of ground-based CMB experiments (so-called Stage-III) plan to field roughly 10^4 polarization sensitive detectors, and the CMB community is actively planning a future Stage-IV effort to field 10^5 - 10^6 detectors,² many of which may populate the focal planes of a small number of high-throughput telescopes.³

Present Stage-III ground-based efforts include Advanced ACTPol (AdvACT) on the six-meter Atacama Cosmology Telescope (ACT),⁴ BICEP3/Keck Array,^{5,6} CLASS,⁷ the Simons Array,⁸ and SPT-3G on the South Pole Telescope⁹ (balloon-borne experiments underway include EBEX¹⁰ and SPIDER,¹¹ and planned satellite missions include LiteBIRD¹²). All of these experiments are fielding, or plan to field, large ($> 10^3$ pixels/array) sub-Kelvin arrays of TES bolometers. Broadly, these experiments seek to map the microwave sky ($\sim(30\text{-}300)$ GHz) in both intensity and polarization on arcminute scales to several degree angular scales to improve our understanding of cosmology, the evolution of structure in the universe, galaxy clusters, and millimeter sources. High signal-to-noise polarization maps over degree angular scales in particular have the potential to provide unique sensitivity to the signatures of gravitational waves produced in the very early Universe, such as those produced in some inflationary models.¹³

The readout of these large sub-Kelvin detector arrays is complex, requiring novel superconducting electronics with thousands of components and interconnects. To reduce the cost and complexity of the readout and the thermal load on the cryogenics presented by warm electronics and cables, the detectors on these arrays must be multiplexed, with many groups of detectors read out and controlled by a much smaller number of wires and devices. In this proceedings, we describe the implementation and testing of the custom readout developed for the first AdvACT high frequency (HF) array, which consists of 2024 TESes operated at ~ 100 mK.

In §2 we describe the AdvACT experiment. In §3 we discuss multiplexing generally and then the specific multiplexing implementation chosen for AdvACT in §4. In §5, we describe screening and characterization performed on readout components for the first AdvACT array, and we conclude in §6 with a discussion of the implications of this work for future efforts.

2. ADVANCED ACTPOL

AdvACT is a receiver upgrade for the Atacama Cosmology Telescope (ACT) which builds on the success of the Atacama Cosmology Telescope Polarization-sensitive receiver (ACTPol).¹⁴ ACTPol observed with three arrays of TES bolometers in two frequency bands centered at 90 and 150 GHz from 2013 until 2016¹⁵ from the Atacama desert in Northern Chile. AdvACT aims to map roughly half of the microwave sky from the ground in five frequency bands with four upgraded arrays of TES bolometers.⁴ A high frequency (HF) array will observe simultaneously at 150/230 GHz, two medium frequency (MF) arrays will observe simultaneously at 90/150 GHz, and one low frequency (LF) array will observe at 28/41 GHz. The AdvACT arrays will be deployed as a staged upgrade of the existing ACTPol receiver, and the first deployed array will be the HF, which will replace the first ACTPol array in mid-2016.

Each array is fabricated on a single monolithic 150 mm wafer,¹⁶ enabling much denser pixel packing than achievable in the ACTPol arrays which were composed of tiles fabricated on 3" wafers. The higher pixel density of the AdvACT arrays, coupled with the fact that multichroic arrays have twice as many detectors per pixel, nearly doubles the number of detectors in the HF and MF arrays relative to the ACTPol arrays. The ACTPol readout was limited to a maximum of 1024 channels per array, which is far short of the 2024 channels required for the AdvACT HF array. This limitation necessitated a new cryogenic multiplexing architecture (Sec §3), as well as new cryogenic interfaces, electronics, and software (Sec §4).

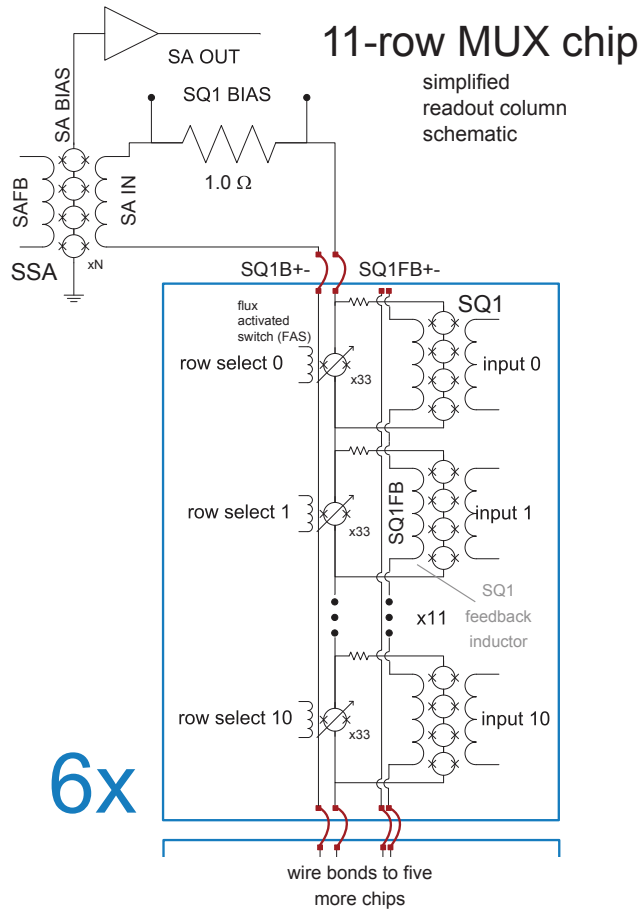


Figure 1. Schematic of the SQUID-based multiplexing circuit used to read out one of the 32 columns of 64 TESes in the AdvACT HF array.²³ Each TES is inductively coupled to its own first stage SQUID series array (SQ1). Each SQ1 is shunted by a flux activated switch (FAS). Each of the 64 SQ1/FAS pairs are connected in series to form the 64 rows. Each row is sequentially addressed by driving its FAS with the flux required to drive it normal, resulting in an approximate voltage bias of its companion SQ1 (when normal, $R_{FAS}/R_{dyn}^{SQ1} \sim (3-7)^{23}$). Channels not being read out are decoupled from the circuit by applying a flux for which their FASes remain superconducting, shorting the inputs of their SQ1s. Each column's SQ1/FAS chain is biased in parallel with a $1\ \Omega$ bias resistor and read out through a $\sim 1\ \text{K}$ SQUID series array (SSA) by the warm preamplifier chain of the Multi-Channel Electronics (MCE).^{24, 25} The TESes are read out by the MCE in a flux-locked loop (FLL) which serves the output of the SSA by means of the SQ1 feedback to maintain linearity in the SQUID readout chain. Each readout column is implemented with six 11-row multiplexing (MUX) chips, only the first of which is shown here. On each column six MUX chips are connected in series using superconducting aluminum wirebonds for 66 rows in total, although only 64 rows are needed to fully channelize the AdvACT HF array. The SQ1 bias and feedback circuits are closed by means of superconducting Al shorting wirebonds at the end of each column (not shown).

3. MULTIPLEXING OVERVIEW

Multiplexing, which enables the readout of a larger number of signals than the number of signaling lines, is a necessary step in the readout of large arrays of cryogenic detectors. Several schemes exist for multiplexing the signals from large arrays of TES bolometers. At present, the most mature techniques employ superconducting quantum interference device (SQUID) amplifiers arranged in Frequency- or Time-Division Multiplexing (FDM¹⁷ and TDM¹⁸) architectures. In TDM, each TES bolometer is sampled sequentially at MHz frequencies, while in FDM, the signal from each TES bolometer is modulated with a carrier wave at a unique frequency (in the MHz) and then demodulated in warm electronics to extract each detector's individual signal. The multiplexing factor (MUX factor) is defined as the number of detectors per readout channel. MUX factors as high as 40 have been achieved on fielded TES arrays by SCUBA2¹⁹ using TDM and as high as 16 by EBEX²⁰ using MHz FDM. Next generation readout systems are in development for CMB experiments utilizing MHz FDM that will operate with MUX factors as high as 64,²¹ as well as TDM systems with MUX factors as high as 128.²²

3.1 SQUID Electronics

The AdvACT arrays will be multiplexed using a new low-frequency TDM architecture with two stages of SQUID amplification. Figure 1 shows a schematic of the multiplexing circuit (MUX). Each TES in the array is inductively coupled to its own first-stage DC SQUID series array (SQ1). The series array is connected in parallel with a Josephson junction array in the form of a Zappe interferometer²⁶ which acts as a flux-activated switch (FAS). Each SQ1/FAS pair forms a channel of the readout, with many channels connected in series to form "columns" of channels. A bias current is applied to the chain of SQ1s/FAS units on each column in parallel with a $1\ \Omega$ resistor. The dynamic resistance of the SQ1/FAS chain is large compared to $1\ \Omega$, so it is approximately voltage

biased. All but one FAS are left in the superconducting state, so that the current does not pass through their companion SQ1s. One FAS associated with the addressed channel is flux-biased in its normal state, so that the full voltage is dropped across that SQ1/FAS unit. Each column of the multiplexer is read out by a unique SQUID series array at ~ 1 K, which provides a second stage of amplification before the warm electronics. Channels are switched across columns by connecting the addressing coil of each FAS in series with one other FAS in every column, forming “rows” of channels.

The AdvACT HF MUX is implemented on 32 columns and 64 rows using this architecture. Variants of the architecture have been used successfully, albeit with lower MUX factors, to read out arrays of X-ray TESes²³ as well as a 1280-pixel array of TESes observing the CMB at 95 GHz in BICEP3.²⁷ Early implementations have shown significant advantages over the three-stage SQUID architecture used in ACTPol, including higher bandwidth, lower power dissipation, and a reduction in total readout noise for comparable MUX factors.²³

4. ADVANCED ACTPOL READOUT IMPLEMENTATION

In order to be read out, each TES in the HF array must be electrically connected to the MUX, and then to the warm readout electronics. §4.1 and §4.2 below describe the custom interfaces developed to interface each AdvACT array with the warm electronics, while §4.3 and §4.4 describe the warm electronics and their operation.

4.1 Cold Electronics and Interfaces

While AdvACT reuses several of the cryogenic interfaces and PCBs from the ACTPol arrays, the new MUX architecture and 150 mm wafer format necessitated a total redesign of the 100 mK PCBs and interfaces for the HF array. Figure 2 shows the focal plane of the integrated HF array. In contrast to ACTPol’s folded vertical readout design,²⁸ the entirety of the new AdvACT 100 mK readout is planar.

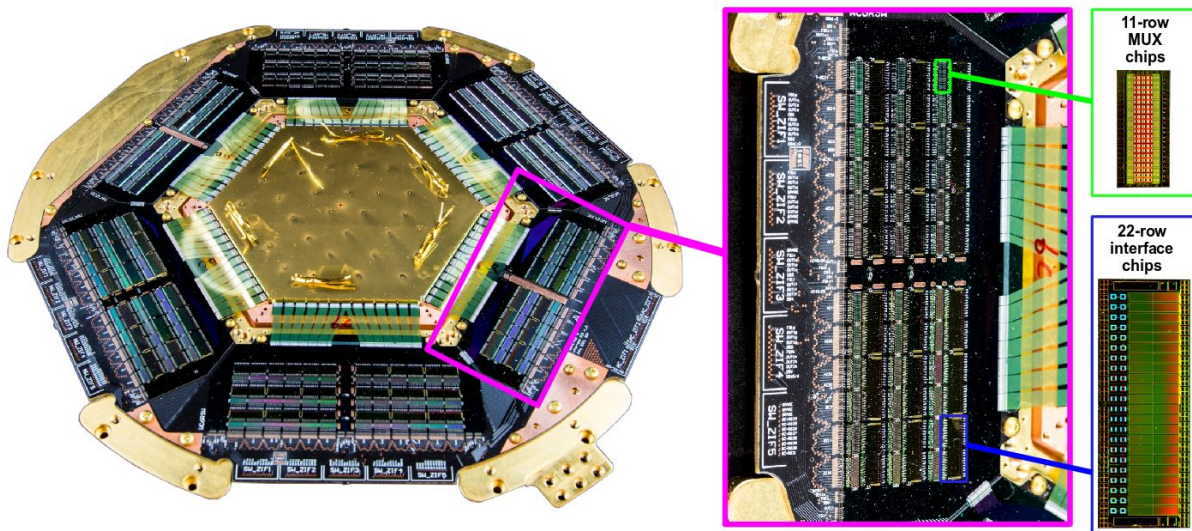


Figure 2. *Left:* The fully integrated AdvACT HF focal plane, pre-deployment. Viewed from the back side of the array package. The hexagonal array, at center, is connected to eight large silicon wiring chips through superconducting flex cables. The wiring chips are glued to the surface of a black ring-shaped PCB mounted to a gold-plated Cu support ring, which interfaces the array and cold electronics with ACT’s dilution refrigerator’s 100 mK cold-plate. *Right:* A closeup of one of the largest silicon wiring chips used to read out the AdvACT HF array, implementing six columns of the 64-row readout. Closeups are also shown of the MUX and detector bias interface chips used to read out the array TESes which are affixed directly to the surface of the wiring chips. Each readout column requires six 11-row MUX chips and three 22-row interface chips.

Each of the 503 feedhorn-coupled pixels in the HF array contains four TESes, with two coupled to orthogonal polarization signals in the 150 GHz band, and the other two coupled to orthogonal polarization signals in the

230 GHz band.²⁹ Three additional pixels at mid-radius in the HF array are not coupled to feedhorns, allowing for dark measurements on those pixels' 12 TESes and mechanical support. Signals from the TESes are connected from each pixel to pairs of bondpads on the edges of the array using between 0.2 and 6.3 cm of 5 μm wide niobium microstrip lines. This results in 338 pairs of bondpads on each side of the array. The pads are 120 μm wide and 400 μm long and arranged into two rows, with an adjacent pad pitch of 140 μm . Each side of the array receives only the signals from one optical band, and orthogonal polarizations within each band for the same pixel are routed together on adjacent microstrip lines to adjacent pad pairs.

From the pads on the sides of the array, the TES signals are connected into custom superconducting flexible cables (flex) developed originally for ACTPol³⁰ with superconducting aluminum wirebonds. Each flex cable is 2 cm long and routes the TES signals through 50 μm wide superconducting aluminum traces on a 70 μm pitch over a flexible polyimide substrate. Each flex cable has thick integrated 5 mm long silicon stiffeners at either end. One stiffener is rubber-cemented to the silicon "wings" attached to the HF array,^{31,32} while the other is rubber cemented to a large readout PCB with a hexagonal inner cut-out. Each side of the flex contains wirebond pads with the same dimensions and pitch as the pads on the array.

From the flex, the TES signals are aluminum wirebonded to a matching set of niobium pads on large silicon wiring chips that are rubber cemented to the PCB and abut the ends of the flex. The eight wiring chips on the PCB that interface with the flex further route the TES signals to bond pad pairs aligned with input pads on the sides of the MUX and interface chips (see Figure 2). Signals are routed on the wiring chips through 0.9 to 5 cm long pairs of 15 μm wide niobium lines on a 30 μm pitch. Four large (10.5 cm x 4 cm) wiring chips are used to route signals to six columns of the MUX apiece, while four smaller (4.9 cm x 3 cm) wiring chips are each used to route signals to two columns of the readout. In order to pack the readout as densely as possible, TES signals are interleaved between MUX and interface chips on each wiring chip, with orthogonal polarization pairs from the same pixel always routed side-by-side into the same readout column together. In this way, detectors in the same pixel observing orthogonal polarizations in the same optical band are read out through the same amplifier chain, on neighboring rows.

The MUX and interface chips fabricated at NIST/Boulder are epoxied to the wiring chips and implement the first stage of the MUX. TES signals are first wirebonded from the wiring chips into a 22-channel bias interface chip (5 mm x 13.45 mm), which connects the TES in parallel with a cryogenic shunt resistor ($\sim 0.2\text{ m}\Omega$) and in series with an optional bandwidth-limiting "Nyquist" inductor.³³ The TESes are then each connected via a pair of wirebonds from each channel of the interface chips to a channel on an 11-channel MUX chip (3 mm x 6.6 mm, see Figure 1) containing the SQ1 and FAS for each TES. The NIST interface chips and MUX chips (NIST mask name "mux15b") are designed to be connected in series, which for the HF readout requires three interface chips and six MUX chips per readout column. One of the extra rows is connected to a row of "dark SQUID" (DSQ) channels threading the MUX that are not connected to TESes and can be optionally read out, while the other spare row is left unconnected. In addition to this optional DSQ row, there are 24 individual channels without detectors scattered throughout the MUX that are also designated DSQ channels and will be read out with the array.

Along the outer perimeter of the PCB, on the edges of the wiring chips, additional aluminum wirebonds distribute SQ1 bias and feedback lines, TES bias lines, and the 64 FAS addressing lines from the PCB into the appropriate MUX and interface chips through additional niobium wiring on the wiring chips. There is one independent SQ1 feedback and SQ1 bias line for every one of the 32 readout columns, but only 24 TES bias lines for the entire array. Although each column in the readout does not have a dedicated TES bias line, each bias line is connected only to TESes in the same optical band, motivated by the significantly different bias conditions expected due to predicted differences in atmospheric loading at 150 and 230 GHz. Five adaptor PCBs connected to the large array PCB through copper flexible cables with zero insertion force (ZIF) connectors distribute the SQUID and TES control lines into PCBs anchored at 1 K through NbTi cables.

The PCBs at 1 K contain the final stage of SQUID amplification and further route the amplified signals, as well as the other SQUID and TES control lines, through superconducting NbTi and low thermal conductivity manganin twisted-pair cables to room temperature electronics which control the multiplexing.^{24,25} The final 1 K SQUID stage is implemented using compatible NIST/Boulder SQUID Series Array Modules (SSAMs).²³ Each SSAM contains eight SQUID series arrays, each of which amplifies a unique readout column in the HF array.

The 1 K AdvACT PCBs are functionally identical to those used in ACTPol, except for the new SQUID series arrays, which have been tailored to work with the 100 mK MUX chips in the new two-stage TDM architecture, and different resistances for cryogenic bias resistors on the SQ1 bias lines.

4.2 Nyquist inductance optimization

The signal from each TES in the array is routed through an interface chip before being inductively coupled into a SQ1. Which pads are bonded on the interface chip for a channel determine how much extra inductance is added in series with each array TES. The purpose of this optional extra inductance is to bandwidth limit the signals from the TES above the Nyquist frequency of the MUX. The planned HF multiplexing rate is 7.8 kHz, although timestreams will be further downsampled to ~ 400 Hz. While the TESes exhibit non-negligible current noise at 10 kHz, the TES bandwidth cannot be arbitrarily restricted with a series Nyquist inductance without jeopardizing the stability of the device, particularly when operated low on the transition³⁴ ($\lesssim 40\%$ the normal TES resistance). To allow for the optimization of the Nyquist inductance for each array, the AdvACT interface chips were designed with three wirebond-selectable Nyquist inductance options realized by N-turn spiral inductors: 0-turn (no added inductance), 9-turn (~ 60 nH of added inductance) and 17-turn (~ 200 nH of added inductance).

Single pixel noise measurements indicate a modest reduction in measured noise (4-10%) for devices connected in series with a 9-turn inductor versus no inductance when multiplexed at 7.8 kHz. Conversely, a visual examination of time streams multiplexed at 250 kHz indicated the onset of instability higher on the transition for identical devices connected in series with the 17-turn inductor, compared to the 9-turn inductor. Example current noise spectra through the superconducting transition for a prototype HF TES are shown in Figure 3. While the TES designs for the two optical bands are different, both exhibited these general trends in noise and stability, leading to the choice of the ~ 60 nH inductance as the target for every TES in the HF array.

Unlike single pixel measurements, TESes in the actual HF array have additional inductance sourced by the extra wirebonds, wiring, and cables connecting them to the interface chips. In a cooldown of a prototype HF array with a quarter of the readout fully populated, we directly measured this additional inductance by comparing the time domain response of the TES bias circuit to square pulses with the TESes superconducting between the prototype array TESes and the single pixel devices. These measurements imply the extra wiring in the array and array readout adds the equivalent inductance of an ~ 8 -turn spiral inductor. Estimates of the added series inductance of the array and readout wiring of 23–100 nH obtained using the FastHenry inductance solver³⁶ are in excellent agreement with (44 ± 28) nH, the measured average and rms inductance for all detectors in the partially integrated HF array prototype. The expected added inductance for each channel depends on the specific length of the wiring connecting it from the array into the readout. Because the array and readout wiring itself on average adds the targeted inductance needed to bandwidth limit the TES signals while maintaining TES stability, the HF interface chips have been bonded so they add no extra inductance.

The series inductance of this wiring bandwidth-limits the TES signals and helps to prevent excess TES noise at frequencies above the multiplexing rate from aliasing into our science band. However, an unavoidable source of noise in any TDM readout is out-of-band SQUID and preamplifier noise above the multiplexing rate, which is aliased into the signal band. This noise source can be mitigated by increasing the multiplexing rate, thereby decreasing the amount of noise power above the Nyquist frequency which can be aliased into the science band. For ACTPol, t_{dwell} , the amount of time the multiplexer spends on each row while switching and sampling, was limited to $\gtrsim 2$ μ s, limiting the multiplexing rate to $\lesssim 15.15$ kHz. Measurements of the total AdvACT readout bandwidth shown in Figure 3 indicate that we still require $t_{\text{dwell}} \gtrsim 2$ μ s, despite the much higher demonstrated bandwidth ($t_{\text{dwell}} = 160$ ns) of the newer MUX architecture.²³ This is of particular concern for the AdvACT HF array which has nearly twice as many channels as the ACTPol arrays, limiting the maximum multiplexing rate to 7.8 kHz. While preliminary data indicates that readout performance at 7.8 kHz will be sufficient to meet AdvACT's science goals, work is underway to increase the bandwidth of the readout chain in order to enable higher multiplexing rates for AdvACT and future efforts.

4.3 Multi-Channel Electronics

Originally developed for SCUBA2,¹⁹ the ambient temperature Multi-Channel Electronics (MCE) used to multiplex the AdvACT arrays have been described extensively elsewhere,^{24, 25} so we focus on the changes that were

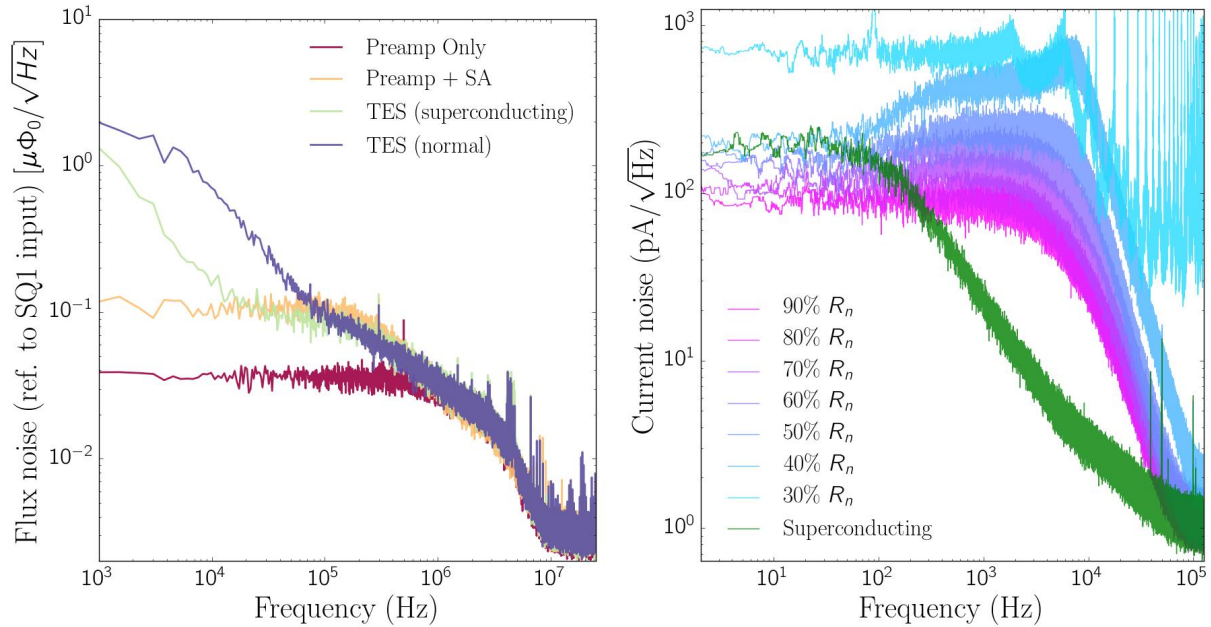


Figure 3. *Left*: Open loop noise measurements taken on a testbed built to match the fielded AdvACT readout illustrating the bandwidth of successive stages of the multiplexer, including the warm MCE preamplifier chain (Preamp). Data were sampled at 50 MHz, and the noise amplitude has been referred to flux at the input coil of the first-stage SQUID. The analog open-loop bandwidth of the multiplexer limits the multiplexing rate to 7.8 kHz for the AdvACT HF array, despite the much higher demonstrated bandwidth of the MUX architecture.²³ At these very high sampling rates, the flux noise due to the superconducting/normal TES is heavily suppressed by the TES bias circuit. *Right*: Current noise measurements taken through the superconducting transition for a prototype HF 230 GHz AlMn TES fabricated on a single pixel test die³⁵ connected to the MUX through a 9-turn Nyquist inductor and operating at a bias power corresponding to the best expected observing conditions in the field, sampling at 250 kHz. These measurements and similar measurements performed on 150 GHz HF devices were used to inform the final TES designs as well as the selected Nyquist inductances for all HF channels. This particular prototype device exhibits detector instability low on the transition ($R_{\text{TES}} \lesssim 40\% R_n$).

required to enable the readout of the AdvACT arrays. Each array is read out using one MCE control crate, and each MCE crate contains nine cards; one addressing card (AC), three bias cards (BCs), four readout cards (RCs), and one clock card (CC). The AC contains 41 digital-to-analog converters (DACs) for switching rows in the MUX, each BC contains 32 DACs for setting and switching SQUID biases and feedbacks, the RCs implement the flux-locked loop (FLL) used to maintain SQUID linearity and read out the TESes, and the CC serves as an interface to and master for each MCE. The BCs additionally source low noise TES bias lines for the arrays.

Only minor firmware modifications and no hardware adjustments to the MCE were required to extend the MUX factor from 33 in ACTPol to 64 for AdvACT. This was possible because of the reduction in signaling lines required by the new two-stage SQUID MUX architecture. ACTPol's three-stage SQUID MUX architecture required independent DACs to specify biases and feedbacks for not only a first stage SQ1 and a 1 K SA, but also for an intermediate second-stage SQ2 on every readout column. While the two-stage architecture requires additional DACs for switching the FASEs on each row, it frees 64 DACs by eliminating the SQ2, 32 of which are used in AdvACT to bias SQ1s, and 32 of which are used to switch additional rows. This results in a total of 33 rows switched from the AC as in ACTPol, and 32 additional rows that can be switched using a BC. While all 65 of these AC and BC DACs are wired to FASEs for the HF array, due to firmware limitations only 64 can be multiplexed simultaneously. One special DSQ row in the multiplexer connected to channels that are deliberately not connected to detectors will not be read out in normal operation.

We have developed software transparently implementing this “hybrid” switching scheme across the DACs of the AC and one BC. While in principle TDM MUX factors as high as 73 should be achievable using MCE

hardware and this hybrid switching scheme, going beyond 64 rows would require significant firmware development to overcome hard-coded limits to the size of memory blocks on the FPGAs of all the MCE cards.

In the old ACTPol MUX architecture, rows in the readout were activated by switching the SQ1 bias “on” to a single fixed value for every SQ1 in that row. One of many benefits of the new architecture is that the SQ1 bias can now be varied at the multiplexing rate ensuring that each SQ1 is individually and optimally biased for each row read out. As in the older architecture, the series array feedback is also independently multiplexed with the array, enabling each of the 2048 HF readout channels to be independently servoed to its own optimal SA operating points.

As in ACTPol, for AdvACT synchronization of data will be accomplished using a “sync box” which provides timing signals to all MCEs and the telescope housekeeping system, allowing bolometer and pointing information to be precisely aligned.³⁷ To allow the telescope to operate with MCEs in both 64 and 33 row configurations for the deployment of the HF array alongside two ACTPol 33-row arrays, the sync box firmware has been altered to provide two, precisely synchronized timing parameter streams. The pointing information is precisely aligned with one of the MCE streams, and for the other MCE stream the pointing is obtained by interpolation.

4.4 SQUID Tuning Procedure

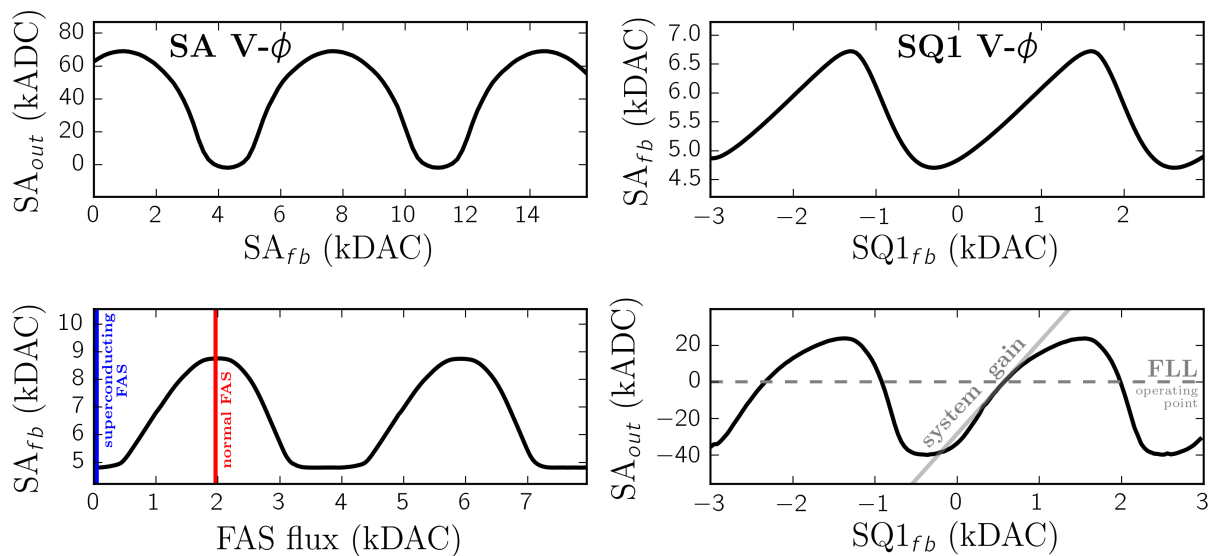


Figure 4. Plots of several stages of the MCE SQUID tuning procedure for the AdvACT HF array, for one example channel. *Upper left:* SQUID Series Array (SA) $V-\phi$ curve, generated by ramping current through the SA feedback coil and directly measuring the SA output voltage with the SA biased at I_c^{max} . *Lower left:* The “FAS servo” tuning stage, generated by ramping current through the FAS flux coil for this channel and measuring the required SA feedback to keep the SA locked. The flux at which the FAS is superconducting (normal) is determined from the minima (maxima) of this curve, and is used to switch channels off (on) while multiplexing the array. *Upper right:* The “SQ1 servo” tuning stage, generated by ramping current through this channel’s SQ1 feedback inductor and measuring the SA feedback required to keep the SA locked, providing a measurement of this SQ1’s $V-\phi$. *Lower right:* The “SQ1 servo” tuning stage, generated by ramping the SQ1 feedback for this channel with the SQUIDs unlocked, provides a sanity check of the detector servo operating point and a measure of the total readout system gain.

We have extended the automated software “tuning” procedure for determining the best operating SQUID biases and feedbacks for the MCE to the AdvACT MUX architecture. Over 10,000 parameters must be chosen to multiplex the full HF array with the MCE, and full automation of the procedure is critical to reduce deadtime due to tuning during observations. Tuning proceeds in stages and builds heavily upon the extensive MCE software tools already developed for ACTPol and other instruments.²⁵ Operating parameters are determined from measuring the $V-\phi$ curves of each SQUID in the MUX, where ϕ is the flux coupled into each SQUID by

ramping current down its feedback coil. Measured $V-\phi$ from different stages of a typical tuning are shown in Figure 4, along with some of the inferred operating parameters.

As for the old architecture, the $V-\phi$ of the 1 K SA is measured first, to determine the optimal SA bias and operating point for each readout column (this tuning stage is described in more detail in a prior proceedings²⁴). The SA operating point for each column is an SA feedback bias at which the SA $V-\phi$ is approximately linear and the measured SA voltage at that feedback is V_{SA} . During FLL operation the SA is held fixed at V_{SA} . This is accomplished by adjusting the total flux coupled into the SA (either directly via the SA feedback, or indirectly via the feedback of a lower coupled SQUID stage) to maintain the output voltage of the SA at V_{SA} .

Next, the FAS “on/off” bias conditions are found as follows. The SA feedback required to return the SA output voltage to V_{SA} is determined as the FAS flux is ramped. This SA feedback is proportional to the total current through the FAS and SQ1. The FAS servo curves typically show ranges of FAS flux over which the FAS response is flat and the FAS is superconducting, and ranges of FAS flux over which the FAS exhibits a finite voltage drop, and is resistive, voltage biasing its companion SQ1. Because the FASes are superconducting for zero applied flux, the FAS superconducting (normal) flux is chosen as the first minimum (maximum) of these FAS flux ramp curves. These flux values are stored and the MUX begins switching, sequentially setting each row to be readout to its normal flux while pinning all other rows to their superconducting flux values.

Following the FAS servo stage is an “SQ1 servo” stage, identical to the former except that the SQ1 feedback is ramped instead of the FAS flux. This is done while the FASes are being switched, resulting in per-channel SQ1 $V-\phi$ measurements, which are repeated over a range of pre-specified SQ1 biases. The SQ1 servo stage allows the determination of the optimal SQ1 bias that maximizes the peak-to-peak modulation of each channel’s SQ1 $V-\phi$ for 2048 SQ1 bias values in total. In addition to an SQ1 bias for each channel, this stage determines the SA feedback required to run each channel at the SA operating point. The MUX then begins switching the per-channel SA feedbacks and SQ1 biases to their optimal values in preparation for array readout.

The last stages of the tuning, besides initiating the TES FLL, maps the open loop response of each channel by ramping the SQ1 feedback and measuring the output SA voltage. The data taken in this “SQ1 ramp” stage provide a sanity check for the configuration of every MUX channel, and can be used to better optimize the tuning servos used in the FAS servo and SQ1 servo tune stages. A similar “SQ1 Ramp TES” diagnostic tuning stage measures the open loop response of the MUX to ramping the voltage on all TES bias lines simultaneously and can be used to optimize the FLL used to measure the TES signals.

5. HF READOUT COMPONENT CHARACTERIZATION AND SCREENING

In total, 96 interface chips, 192 MUX chips, and more than 20,000 aluminum wirebonds are required to fully channelize the 2024 TESes in the HF array. Below, we discuss the screening performed on all of the MUX and interface chips integrated into the AdvACT HF array. More details on the integration of the HF array and its many components can be found in accompanying papers in this proceedings.^{31,32}

5.1 MUX chip screening data and analysis

For screening, multiplexing chips are assembled on an independent test PCB in eleven columns of four chips each. The chips are tuned in stages as described in §4.4 above, optimizing the parameters required by each stage. Once optimized, a full tune is taken at an SQ1 bias close to the expected optimal bias and the data from each stage of the tuning are examined individually to flag critical failures (open lines, unresponsive SQUIDs, etc.). Next, full tunes are taken on each readout column individually, slightly incrementing the SQ1 bias current for each successive tune to map each SQ1’s $V-\phi$ modulation as a function of SQ1 bias. At low SQ1 bias, no modulation occurs. There is an intermediate range of SQ1 biases where the SQ1 $V-\phi$ curves show modulation, but still have a superconducting branch. At sufficiently high SQ1 bias, the superconducting branch disappears.

The critical current I_c^{min} is the smallest current applied to the SQ1 bias for which modulation appears. The critical current I_c^{max} is the current for which the superconducting branch of the SQ1 $V-\phi$ curve first completely disappears. Here, I_c^{min} and I_c^{max} are defined as stated when the FAS is normal. For this first SQ1 bias sweep, the SQ1 bias is stepped between tunes by between 73.5 and 294 nA from zero up to $\sim 2.5I_c^{max}$, typically corresponding to steps of 0.5% and 2% of I_c^{max} , respectively (later screens were done at higher resolution in SQ1 bias). I_{FAS}

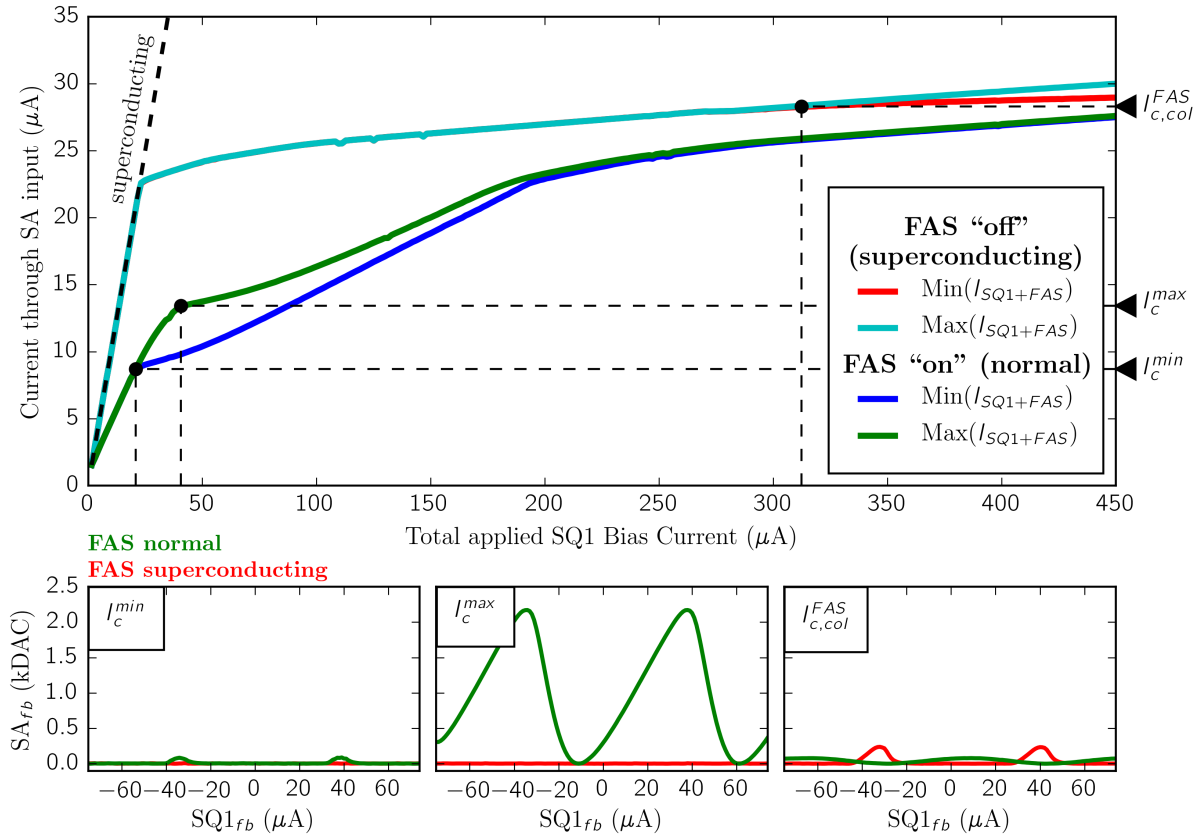


Figure 5. *Top*: The minimum and maximum current through an example channel's SQ1 and FAS, extremized over all values of applied SQ1 feedback, measured from SQ1 servo curves as a function of SQ1 bias. Measurements are shown both with the FAS superconducting (cyan and red) and normal (dark green and dark blue). With the FAS normal (channel on), the majority of the current is shunted through the channel's SQ1. Arrows denote SQ1 biases and currents corresponding to I_c^{min} , where the minimum and maximum current first diverge, and I_c^{max} where the difference is extremized. Also denoted is $I_{c,col}^{FAS}$, the SQ1 bias at which the readout column containing this channel first exhibits persistence. *Bottom Left*: SQ1 servo curves for this channel with its FAS normal (green) and superconducting (red) at an SQ1 bias current just above I_c^{min} . *Bottom Middle*: Same but with the SQ1 bias current at I_c^{max} . At I_c^{max} the channel's SQ1 is no longer superconducting for any applied SQ1 feedback. *Bottom Right*: Same but with the SQ1 bias current just above $I_{c,col}^{FAS}$. At these high SQ1 bias currents, at least one FAS on this channel's readout column is no longer superconducting for any applied flux and the MUX is no longer able to properly switch on this column.

is the amount of current applied to the FAS flux input which switches a particular channel of the MUX on. The goals of the screening are to ascertain if a MUX chip is functioning normally and to determine these three parameters so that we can optimize which MUX chips will be integrated together into readout columns.

The process of taking tunes while ramping the SQ1 bias is then repeated, but this time with coarser steps and a much higher maximal value of SQ1 bias ($\gg I_c^{max}$), and with all FASes switched off. The purpose of this ramp is to check for "persistence" near or below I_c^{max} : a row may remain on for all values of I_{FAS} , interfering with the readout of every other row on a column. Although this is a failure which affects the entire readout column, it is usually possible to identify the offending channel. This is cause to mark a MUX chip defective, and is typically diagnosed by observing an unusual FAS servo tuning curve. If the chip with the persistent channel can be identified, the other chips on the column must be retested in a subsequent cryogenic screening. At very high SQ1 biases ($\gg I_c^{max}$), even channels which do not exhibit persistence at or near I_c^{max} will become persistent. We require that this critical current, $I_{c,col}^{FAS}$, be $\geq 2I_c^{max}$ for the chips on a screening column to be included in the HF array. This additional selection was imposed partway through screening and only approximately one half

of the MUX chips integrated into the HF array satisfied this inequality, although every chip integrated into the array had $I_{c,col}^{FAS}/I_c^{max} > 1$ (only lower limits on $I_{c,col}^{FAS}/I_c^{max}$ were obtained for these chips). Figure 5 illustrates how I_c^{min} , I_c^{max} and $I_{c,col}^{FAS}$ are determined from the aforementioned SQUID current and voltage sweeps.

Other parameters of interest for each MUX channel are determined from the first sequence of tunes versus SQ1 bias with the FASes switching normally. In particular, I_{FAS} for each FAS is determined from the values used in the tune nearest I_c^{max} , since in operation each SQ1 will be biased near its I_c^{max} value.

The algorithms for determining I_c^{min} and I_c^{max} from these data are very similar. First, the minimum (for I_c^{max}) or maximum (for I_c^{min}) of the SQ1 servo curves is determined for each SQ1 bias. Physically, the ordinate of the SQ1 servo curves corresponds to the current through the SQ1 (very little current is sourced by a channel's FAS when it is normal) and is calibrated from SA feedback in digital counts to physical current using the measured DC impedance of the SA and SQ1 cold circuits and the ratio of the mutual inductances of the SA feedback and input coils. The current through the SQ1 varies approximately linearly with SQ1 bias current, if the impedance of the SQ1 loop relative to its $1\ \Omega$ shunt resistor is constant. Discontinuities occur when the impedance in the SQ1 loop changes, as when modulation first appears at I_c^{min} or when the SQ1 superconducting branch first disappears at I_c^{max} , as shown in Figure 5. We determine I_c^{min} and I_c^{max} by identifying the currents through the SQ1 at which these curves exhibit these discontinuities. The actual values of I_c^{min} and I_c^{max} are determined by fitting these curves below and above their corresponding discontinuities to lines and computing the SQ1 current at these lines' intersection points.

5.2 HF MUX chip screening results

After screening, only chips passing the selection criteria are considered for array integration. The majority of chips fail the screening due to wiring errors, dead channels, channels with unusual looking SQUID curves (either FAS or SQ1), a value of $I_{c,col}^{FAS}$ less than $2I_c^{max}$ (for chips screened later), a range of I_c^{max} values among its eleven rows of more than 25% from the chip's mean I_c^{max} , or damage sustained in handling or fabrication. All of the channels on chips that pass these criteria tend to have similar values for I_c^{min} and I_c^{max} , but between these chips these values may vary. In particular, the mean and rms I_c^{max} for chips from the three wafers screened for the HF array, W5, W6 and W7, were $(9.9 \pm 0.6)\ \mu\text{A}$, $(13.5 \pm 0.6)\ \mu\text{A}$, and $(12.8 \pm 0.7)\ \mu\text{A}$, respectively. For passing chips, I_{FAS} values were nearly identical, with a mean and rms of $(240 \pm 14)\ \mu\text{A}$. It is critical for the I_{FAS} of FASes on the same row to be as similar as possible for the channels to switch properly.

Reinhold and Koelle³⁸ give a transcendental equation relating the ratio of I_c^{min}/I_c^{max} to the SQUID screening parameter $\beta_L \equiv 2LI_0/\Phi_0$, where L is the SQUID loop inductance, I_0 is the critical current of each SQUID Josephson junction, and Φ_0 is the magnetic flux quantum. A cross-check to validate our screening procedure is to plot I_c^{min}/I_c^{max} against the parameter β_L and compare it to a numerical solution of the theoretical prediction. Such a plot for each channel on chips which passed the HF screening can be seen in Figure 6. To compute β_L , we assume that $L = 120\ \text{pH}$, the nominal design SQ1 loop inductance.

Chips with similar I_c^{max} values are grouped together on a column for integration. Although the SQ1 bias values are multiplexed, this helps to avoid creating columns where one chip's I_c^{max} is greater than another chip's $I_{c,col}^{FAS}$. Columns for the array were chosen by first sorting screened chips by their I_c^{max} values and then grouping consecutive chips in the sort into 6-chip readout columns.

5.3 HF interface chip screening

A total of 130 interface chips were screened for the HF array, with only 96 chips selected for final integration. Chips were warm probed for shorts between adjacent channels, and the summed resistance of all 22 shunt resistors on each interface chip was measured cryogenically using a four-lead configuration in a dilution refrigerator at 100 mK. Common reasons for an interface chip to fail screening included unintentional shorts between adjacent channels due to fabrication errors and abnormal cryogenic resistance. The target per-channel shunt resistance R_{sh} was $180\ \mu\Omega$. The interface chips in the HF array came from four 3" wafers of 40 interface chips apiece fabricated at NIST/Boulder. The average R_{sh} over three wafers was $203\ \mu\Omega$ with no more than 5% deviation for any measured chip (although one anomalous fourth wafer, W2, had an average R_{sh} of $156\ \mu\Omega$). Chips from all four wafers were integrated into the HF without mixing chips from W2 with chips from other wafers on the same

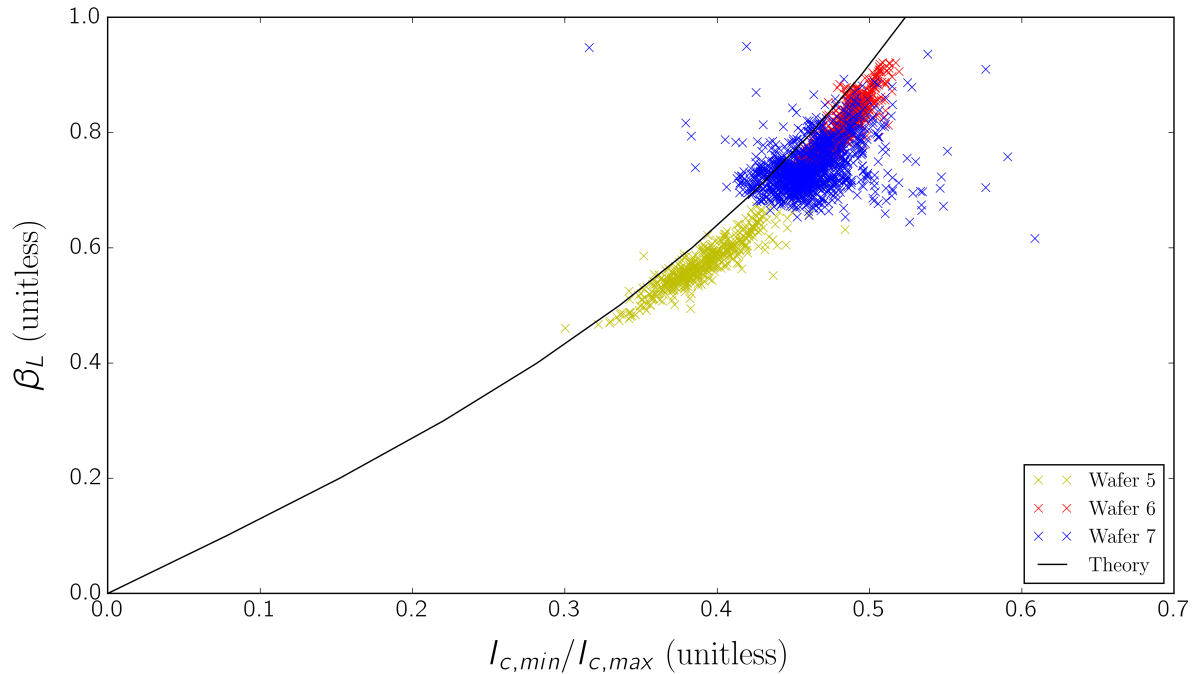


Figure 6. The measured SQUID screening parameter β_L vs I_c^{min}/I_c^{max} for each channel, organized by wafer for MUX chips which passed screening for the AdvACT HF array. Channels which operate as designed are expected to fall along the theory curve, which is a numerical solution to the transcendental equation relating β_L to the ratio of I_c^{min}/I_c^{max} from Reinhold and Koelle.³⁸

TES bias line. Chips were further grouped on each bias line by their measured 100 mK resistances, requiring less than a 3% deviation in total cryogenic resistance for chips on the same TES bias line.

6. SUMMARY

The readout components for the first AdvACT array have been screened, and integration is complete. We have described the design and performance of the readout electronics for the array, and this readout has been used successfully to characterize the AdvACT HF array, which will be deployed in mid-2016 and observe the CMB at 150 GHz and 230 GHz.

The readout techniques developed for AdvACT and described in this proceedings enables the readout of significantly larger arrays of TES bolometers than was previously possible using an MCE. While other multiplexing schemes employing alternate technologies are currently under development and could yield MUX factors an order of magnitude larger than the 64 MUX factor demonstrated here,^{39–41} current efforts that rely on low-frequency TDM to multiplex large arrays of TES bolometers stand to benefit substantially from larger MUX factors.

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